UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,852	12/28/2001	Tommy K. Eng	21192-06625	4831

758 7590 05/03/2004

FENWICK & WEST LLP
SILICON VALLEY CENTER
801 CALIFORNIA STREET
MOUNTAIN VIEW, CA 94041

EXAMINER	
DO, THUAN V	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,852	ENG, TOMMY K.	
	Examiner	Art Unit	
	Thuan Do	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final office action is responsive to amendment entered on 02/20/2004. Claims 3-37 are pending in this office action. Claims 1,2 have been canceled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claim 3-37 are rejected under 35 U.S.C. 102(e) as being unpatentable over Dangelo, Pat. No. 6,216,252.

Regarding claim 3: Dangelo teaches a method comprising :

optimizing a network of logic building blocks logically and physically using placement based information to create an accurate model of the electronic design (col. 8, lines 41-53 using placement modules, col. 9, lines 1-8 with optimizing gate blocks of ASIC and figure 4) ; and

passing optimized design information associated with the accurate model to gate-level implementation tools to achieve predictable results at gate-level implementation of the electronic design (col. 8, lines 41-53, col. 9, lines 1-8, figure 4 and col. 3, lines 3-21 using predicate logic in implementing electronic design).

Regarding claims 4-13: These claims teach well known methods to support claim 3 and rejected in the similar manner.

Regarding claim 14: Dangelo teaches a method comprising:

creating a virtual prototype to model the electronic design thereby enabling design optimization (col. 3, lines 58-67) before detail physical implementation (col. 6, lines 41-55 using frequent simulation of the circuit being designed in small parts before it is simulated as a whole) ; and

deriving a solution for design convergence based on data resulting from the design optimization (col. 4, lines 57-62).

Regarding claim 15: This claim teaches a well known method to support claim 14 and rejected in the similar manner.

Regarding claim 16: Dangelo teaches a method comprising:

mapping (col. 7, lines 63-67) the model into logic building blocks thereby creating a network of logic building blocks, a number of the logic building blocks having a logic structure including a plurality of gates thereby providing a higher level of abstraction than gates (col. 8, lines 41-53, col. 9, lines 1-8, figure 4) ; and

optimizing the network of logic building blocks, each logic building block having performance data based on placed and routed implementations of that logic building block (col. 8, lines 41-53, col. 9, lines 1-8, figure 4).

Regarding claims 17-30: These claims teach well known methods to support claim 16 and rejected in the similar manner.

Regarding claim 31: Dangelo teaches a method with:

clustering multiple logical building blocks into partitions thereby yielding a partition level abstraction of the electronic design (col. 9, lines 1-8 and col. 4, lines 10-20) ;

creating a model for each partition (col. 4, lines 10-20); and

optimizing additional levels (col. 3, lines 43-55) of the electronic design using the partition models thereby enabling hierarchical optimization without reanalyzing partition level details (col. 3, lines 58-67 where Dangelo is silent about reanalyzing partition level details) .

Regarding claim 32: Dangelo teaches a method comprising:

creating physical implementations of a logic building block, the logic building block having a logic structure including a plurality of gates thereby providing a higher level of abstraction than gates (col. 6, lines 41-55 using frequent simulation of the circuit being designed in small parts before it is simulated as a whole) ; and

monitoring (col. 1, lines 61-67) area and performance data of each physical implementation based on a number of selected input parameter sets (col. 3, lines 48-55).

Regarding claims 33,34: These claims teach well known methods to support claim 32 and rejected in the similar manner.

Regarding claim 35: Dangelo teaches a computer program comprising:

a library of logic structures (col. 12, lines 40-55), each logic structure having performance data based on placed and routed implementations of that logic building structure (col. 11, lines 44-55), the performance data being organized according to characteristics of the implementations (col. 4, lines 49-55) ; and

a plurality of modules for optimizing a network of a number of the logic structures using placement based information to create an accurate model of the electronic design thereby enabling optimized design information (col. 3, lines 58-67) associated with the accurate model to be passed to gate-level implementation tools to achieve predictable results at gate-level implementation of the electronic design (col. 8, lines 41-53, col. 9, lines 1-8, figure 4 and col. 3, lines 3-21 using predicate logic in implementing electronic design).

Regarding claims 36,37: These claims teach well known programs to support claim 35 and rejected in the similar manner.

Response to Arguments

3. Applicant's arguments have been considered but they are not persuasive as following response:

Applicant argues that Dangelo does not teach or suggest using placement based information as recited in the pending claims.

The prior art of Dangelo teaches wire delay estimation information for placement of buffers for optimizing logic block design in column 14, line 56 through column 15, line 7 where wire delay information module is performed using the specified requirement of

timing characteristics in column 11, lines 44-55. This information meets the claimed limitation of " optimizing a network of logic building blocks logically and physically using placement based information to create an accurate model of the electronic design ".

The remark's features such as "The performance data preferably quantifies the relationship between the area, circuit delay, and output load of the logic structure for a number of different physical implementations" since they are not in the claim and would not effect the office rejection.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Do whose telephone number is 571-272-1891. The examiner can normally be reached on Monday-Friday 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are 703 305-3431 for regular communications and 703-305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0596.

Thuan Do
Patent examiner
4/28/04